## IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1-6 (Cancelled)

- 7. (Currently Amended) A method comprising:
  - (a) reading a first stream of image pixels corresponding to an image  $X_K$  from an image buffer;
  - (b) reading a second stream of pixels corresponding to an image  $A_K$  from an accumulation buffer;
  - (c) blending each image pixel of the image  $X_K$  with the corresponding accumulation buffer pixel of the image  $A_K$  based on an alpha value provided with the image pixel, and thus, generating a third stream of output pixels defining an image  $A_{K+1}$ ; and
  - (d) transferring the third stream of output pixels to the accumulation buffer;
  - (e) performing (a), (b), (c) and (d) for each image in a sequence of images  $X_K$ , K=0, 1, 2, ..., N-1, wherein N is the number of images in the sequence.
- 8. (Original) The method of claim 7, wherein the accumulation buffer color depth precision is larger than the image buffer color depth precision.
- 9. (Currently Amended) The method of claim 8 [[7]], wherein said blending comprises blending red, green and blue components of each output pixel in parallel.
- 10. (Currently Amended) The method of claim 7, wherein (a), (b), (c), (d) and (e) and (d) are performed by a graphics hardware accelerator chip in response to software

functions executed on a host processor, wherein the image buffer and the accumulation buffer are external to the graphics hardware accelerator chip.

## 11-12. (Cancelled)

- 13. (Currently Amended) The graphics system of claim 23 [[11]], wherein the texture buffer comprises one or more synchronous dynamic RAMs (SDRAMs).
- 14. (Currently Amended) The graphics system of claim <u>23</u> [[11]], wherein the frame buffer comprises one or more 3D-RAM memory devices.
- 15. (Cancelled) The system of claim 1, wherein the first stream of image pixels corresponds to a single image.
- 16. (Cancelled) The method of claim 7 further comprising: blending a plurality of images by repeatedly performing (a), (b), (c) and (d).
- 17. (New) A system comprising:

an accumulation buffer;

an image buffer; and

a mixing unit configured to (a) read a first stream of image pixels corresponding to an image  $X_K$  from the image buffer, (b) read a second stream of pixels corresponding to an image  $A_K$  from the accumulation buffer, (c) blend each image pixel of the image  $X_K$  with the corresponding pixel of the image  $A_K$  based on an alpha value provided with the image pixel, and thus, generate a third stream of output pixels defining an image  $A_{K+1}$ , and (d) transfer the third stream of output pixels to the accumulation buffer;

wherein the mixing unit is further configured to perform (a), (b), (c) and (d) for each image in a sequence of images  $X_K$ , K=0, 1, 2, ..., N-1, wherein N is the number of images in the sequence.

- 18. (New) The system of claim 17, wherein the color precision of the accumulation buffer is greater than the color precision of the image buffer.
- 19. (New) The system of claim 18, wherein the mixing unit includes a plurality of mixing circuits, wherein each mixing circuit operates on a corresponding color component.
- 20. (New) The system of claim 19, wherein the accumulation buffer resides within a texture buffer of a graphics system.
- 21. (New) The system of claim 21, wherein the image buffer resides within the frame buffer of a graphics system.
- 22. (New) The system of claim 18, wherein the color precision of the accumulation buffer is at least  $\Delta N$  larger than the color precision of the image buffer, wherein  $\Delta N$  is the base two logarithm of the maximum number of images to be blended into the accumulation buffer.
- 23. (New) A graphics system comprising:
  - a frame buffer;
  - a texture buffer;
- a hardware accelerator configured (a) to read image pixels corresponding to an image  $X_K$  from the frame buffer, (b) to read pixels corresponding to an image  $A_K$  from an accumulation buffer allocated in the texture buffer, (c) to blend each of the image pixels of the image  $X_K$  with the corresponding pixel of the image  $A_K$  using an  $\alpha$  value of the

image pixel as the blend fraction, and thus, generate output pixels defining an image  $A_K$ , and (d) to transfer the output pixels to the accumulation buffer;

wherein the hardware accelerator is further configured to perform (a), (b), (c) and (d) for each image in a sequence of images  $X_K$ , K=0, 1, 2, ..., N-1, wherein N is the number of images in the sequence.

24. (New) The graphics system of claim 23, wherein the texture buffer has a configurable pixel depth precision.